Jordanian Journal of Computers and Information Technology (JJCIT), Vol. 2, No. 3, December 2016.

A 1.2-V LOW-POWER FULL-BAND LOW-POWER UWB TRANSMITTER WITH INTEGRATED QUADRATURE VOLTAGE-CONTROLLED OSCILLATOR AND RF AMPLIFIER IN 130NM CMOS TECHNOLOGY

Fadi R. Shahroury

Department of Electrical Engineering, Princess Sumaya University for Technology, Amman, Jordan.
fadi@psut.edu.jo

(Received: 10-Feb.-2016, Revised: 11-Apr.-2016, Accepted: 24-Apr.-2016)

ABSTRACT

This paper presents the design and simulation of a low-power full-band UWB transmitter with on-chip quadrature voltage-controlled oscillator (QVCO) in 130 nm CMOS technology. The proposed transmitter consists of a passive poly-phase filter (PPF), QVCO, a quadrature modulator core and an RF power amplifier. The QVCO uses the differential delay cell architecture with four cascaded stages. The transmitter has the following specifications: a 15.28 dB average conversion gain with a ripple of ±1dB from 2 GHz to 11 GHz, the average input 1-dB compression point (IP1dB) is –10 dBm and the average output 1-dB compression point (OP1dB) is 4.35 dBm. The QVCO achieves a wide frequency range (2-11 GHz) with a –80 dBc/Hz phase noise. In addition, the supply voltage of the proposed transmitter is 1.2 V with power consumption of 77.8 mW.

KEYWORDS

UWB, QVCO, Up-conversion mixer, 130 nm CMOS technology.

1. INTRODUCTION

Ultra-Wideband (UWB) technology has been around since the 1980s, but it has been used for radar applications [1], since it gives accurate timing information due to the signal wideband nature. However, the need for high data rate has made short-range UWB wireless communications quite popular. Besides, the UWB is becoming more attractive for low-cost communication applications, because it provides low power consumption, large bandwidth and high data rates (up to 480 Mbps within 10m distance) [2]. Multi-band orthogonal frequency division multiplexing (MB-OFDM) and impulse radio communication are both under the UWB standards. However, the impulse radio approach faces the potential problem of many narrow-band systems co-existing as well as several technical challenges related to generation of short pulses [3]. Thus, overcoming these challenges enhanced the MB-OFDM approach which is used in this work.

So far, a variety of transmitters have been reported to implement MB-OFDM UWB transmitter [3]-[7]. However, scrutiny of these papers revealed that all UWB transmitters proposed have relatively high power consumption, although they did not contain an on-chip QVCO. Besides, they did not

cover the full-band of MB-OFDM (2-11GHz), except the proposed work in [7]. However, the transmitter in [7] is designed with 14 on-chip spiral inductor.

In this paper, a UWB CMOS transmitter for multi-band OFDM applications is implemented using 130 nm CMOS technology with power consumption of 77.8 mW from a 1.2 V supply voltage. The designed transmitter covers the full-band of MB-OFDM (2-11GHz). It consists of a passive poly-phase filter (PPF), a quadrature voltage-controlled oscillator (QVCO), a quadrature modulator core and an RF power amplifier. In addition, only 8 on-chip inductors are used in the proposed transmitter.

This paper presents the design and simulation of a low-power full-band UWB transmitter. The system overview for UWB is discussed in Section 2, the operational principles and the design of the building blocks is addressed in Section 3. The simulation results of the proposed transmitter circuit are reported in Section 4, followed by a conclusion in Section 5.

2. SYSTEM OVERVIEW

MB-OFDM UWB system is a system that enables transmitting data over multiple carriers at precise frequencies at the same time. Multi-band OFDM system consolidates the multi-band (MB) approach with the OFDM modulation technique. This approach divides the spectrum into smaller sub-bands each with a bandwidth greater than 500 MHz (Federal Communications Commission (FCC) requirement for a UWB system) and uses one of the sub-bands in each time-slot to transmit the OFDM symbols. The system is denoted as a UWB-OFDM system since it is an OFDM system, but operates over a very wide bandwidth, much larger than the conventional OFDM system bandwidth.

In order to uphold the UWB standards based on OFDM, the MB-OFDM Alliance (MBOA) was formed in 2003. As stated in the MBOA and WI Media standard [8], the UWB spectrum extends over the frequency range from 3.168 GHz to 10.56 GHz and is divided into 14 bands, each band of which has a bandwidth of 528 MHz and consists of 128 sub-channels, where the bandwidth of each sub-channel is 4.125 MHz. The bands are gathered into five groups, the first four groups consist of three bands, so they contain the first 12 bands, and the fifth one contains the last 2 bands, as illustrated in Figure 1.

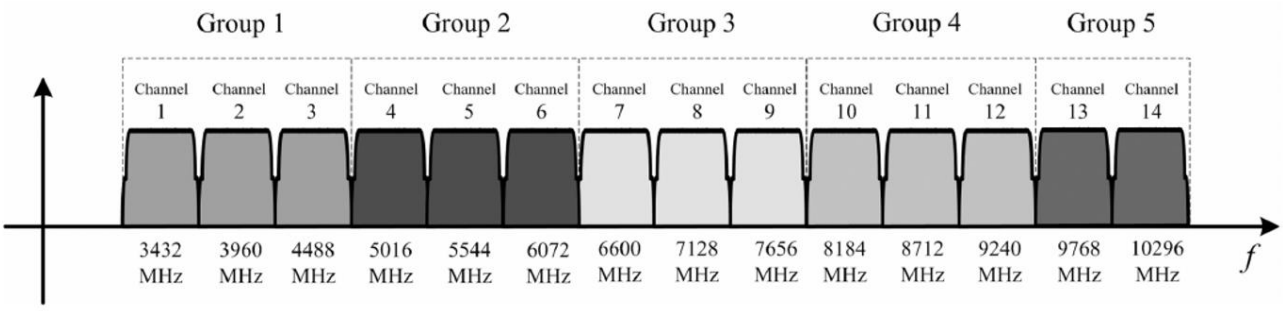


Figure 1. The allocation of the bands in the UWB MB-OFDM system.

3. PRINCIPLE OF OPERATION

Figure 2 shows the block diagram of the proposed UWB transmitter system which consists of a passive poly-phase filter, a quadrature modulator core, a quadrature voltage-controlled oscillator and an RF power amplifier. The quadrature modulator core is formed by two mixers and one adder and converts the quadrature intermediate frequency (IF) signals and the quadrature local oscillator (LO) signals into the single-side-band signal. The quadrature LO signal is obtained from a QVCO which operates from 2 GHz to 11 GHz, and the quadrature of the input IF signal is achieved by the passive poly-phase filter. Then, the amplification of the output signal of the quadrature modulator is carried out using an RF power amplifier, in order to drive the load of the output. For the measurement purpose, the single ended to differential and differential to single ended off-chip transformation at the IF input port and RF output port are used, respectively.

The following subsections describe the operational principles and the circuits' realization of the quadrature modulator core, the PPF, the QVCO and the power amplifier.

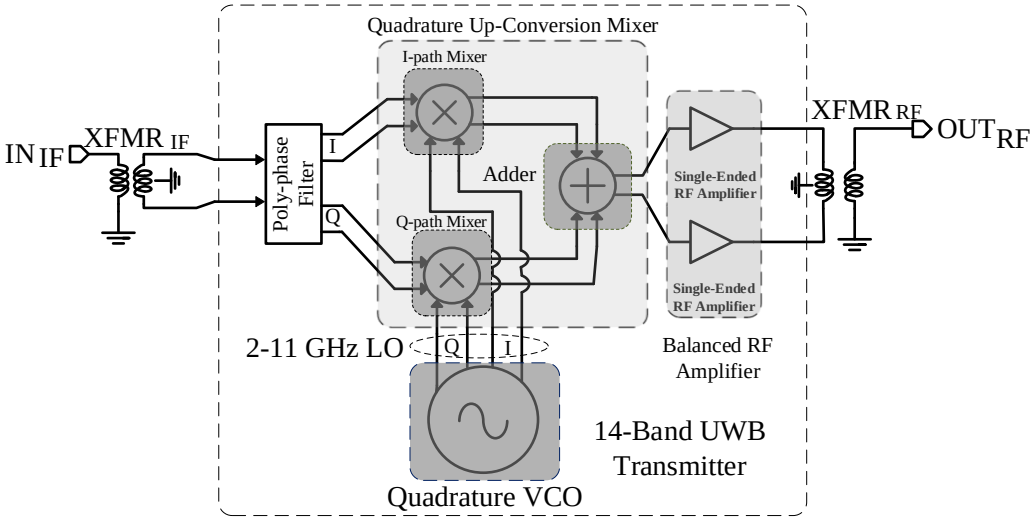
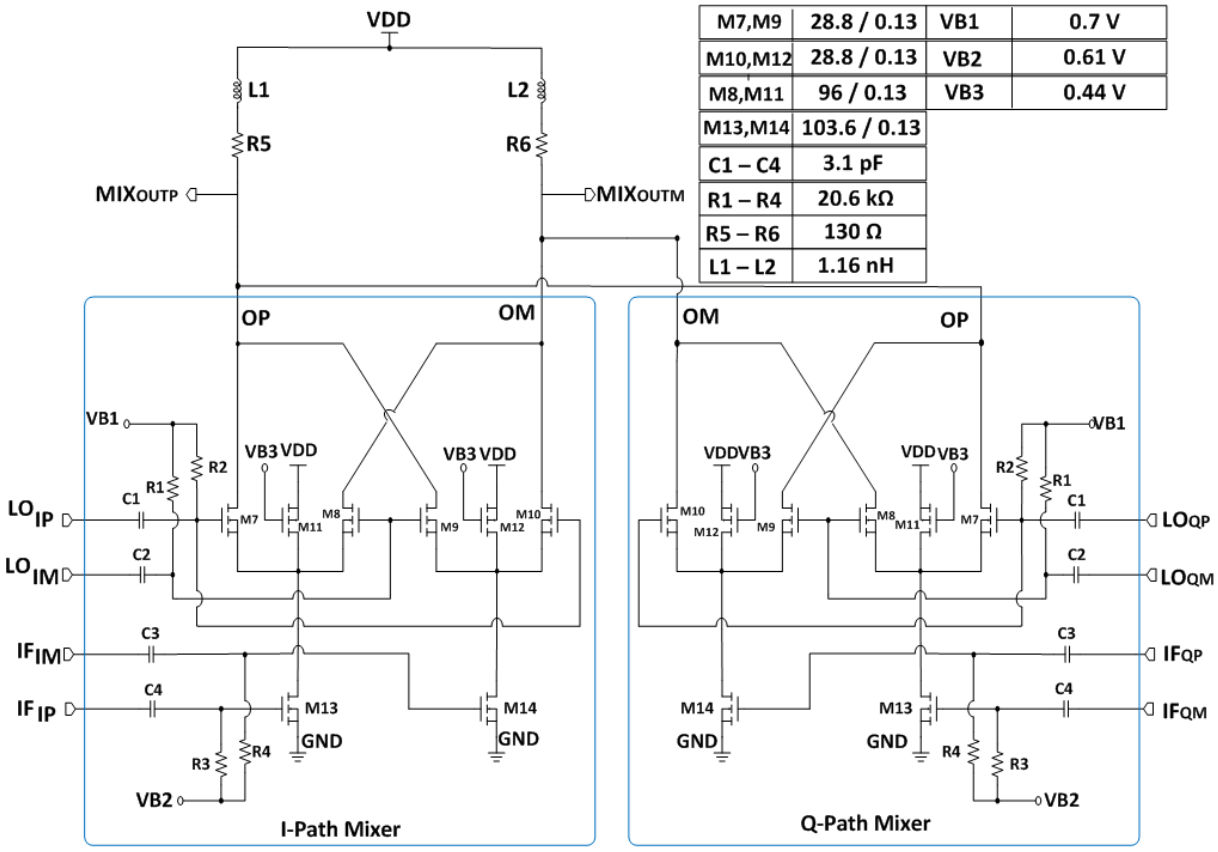


Figure 2. The block diagram of the full-band UWB transmitter.

3.1 Quadrature Modulator Core

Figure 3. shows the schematic diagram of the quadrature modulator core which is composed of two paths: the I-path and the Q-path. The output of each path is added in current domain at nodes OP and OM. Every path contains a double-balanced quadrature up-conversion mixer.

In each double-balanced quadrature up-conversion mixer, transistors M7-M10 form the Gilbert cell core [9], where the LO signal is injected. Transistors M13 and M14 are used at the IF input, while M11 and M12 are used as a current source to enhance the conversion gain of the mixer by realizing bleeding technique. The capacitors C1- C4 are used as DC block capacitors, and resistors R1- R4 are used for biasing. Each mixer consumes 16.72 mA from a 1.2 V power supply. The entire mixer including both paths has a total power consumption of about 40.1 mW.



M7,M9	28.8 / 0.13	VB1	0.7 V
M10,M12	28.8 / 0.13	VB2	0.61 V
M8,M11	96 / 0.13	VB3	0.44 V
M13,M14	103.6 / 0.13		
C1 – C4	3.1 pF		
R1 – R4	20.6 kΩ		
R5 – R6	130 Ω		
L1 – L2	1.16 nH		

Figure 3. Simplified schematic diagram of the quadrature modulator core.

3.2 Passive Poly-phase Filter (PPF)

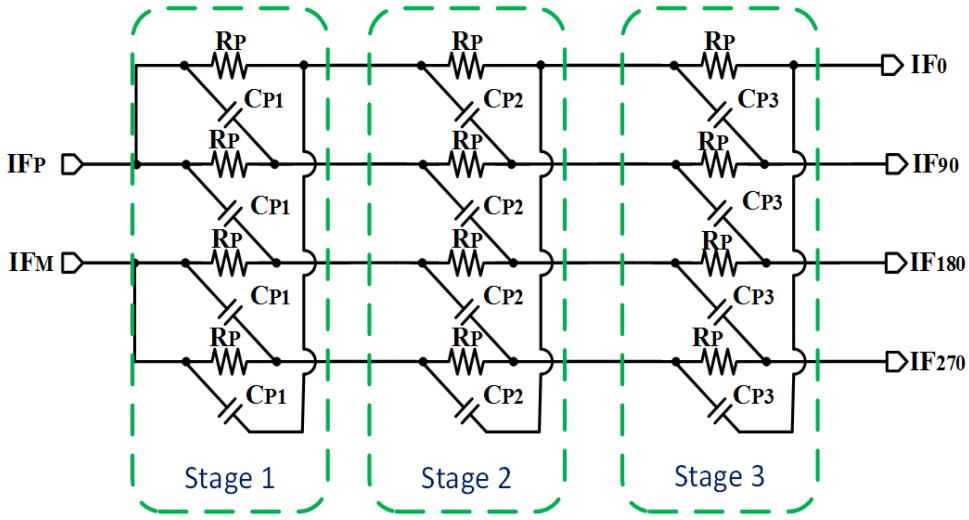
PPF is designed to provide the quadrature modulator core with differential and quadrature inputs, thereby allowing the use of a double-balanced mixer topology. This property proves critical in reducing the LO-to-IF feedthrough. To achieve wider range of operation, three-stage poly-phase RC filter is employed, as illustrated in Figure 4. The unit resistor is 5kΩ in the three-stages, while the unit capacitor is 440 fF, 240 fF and 120 fF in the first, second, and third stage, respectively. To verify the phase precision of PPF outputs, the image rejection ratio simulation methodology is used [10].

3.3 Quadrature Voltage Controlled Oscillator (QVCO)

Figure 5 illustrates the block diagram of the QVCO. A ring QVCO with four differential delay cells is chosen. This structure can effectively reduce chip area and cost as compared to QVCO based on LC ring oscillator structure.

The schematic diagram of each differential delay cell is depicted in Figure 6. In Figure 6, the differential delay cell consists of a differential transistor pair (M3 and M4) with load transistors (M1 and M2) and tail current transistors (M5 and M6). The operation of the QVCO is divided into two modes, high frequency mode (3.28-11.16 GHz) and low frequency mode (1.5-6.2 GHz) based on which tail current transistor (M5 or M6) of the differential delay cell is enabled. In each mode of operation, the oscillation frequency of the ring QVCO is controlled by the gate voltage of M3 and

M4. The designed QVCO based on proposed delay cell covers the frequency range from 2 GHz to 11 GHz and has a phase noise of –80 dBc at 1MHz offset frequency with a power consumption of 19.4mW.



RP	5 kΩ
CP1	440 fF
CP2	240 fF
CP3	120 fF

Figure 4. The circuit schematic diagram of the poly-phase filter.

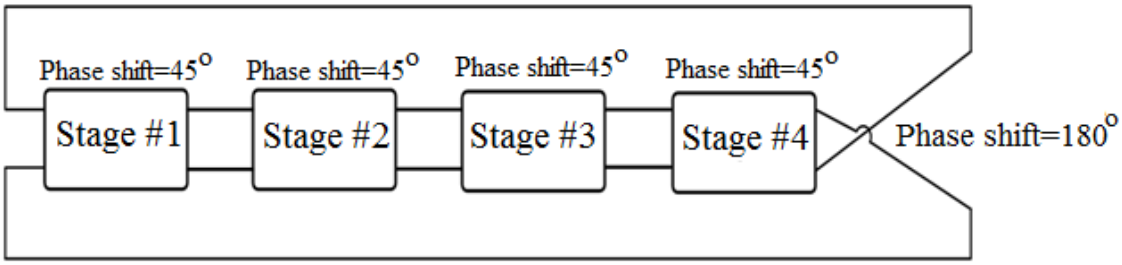
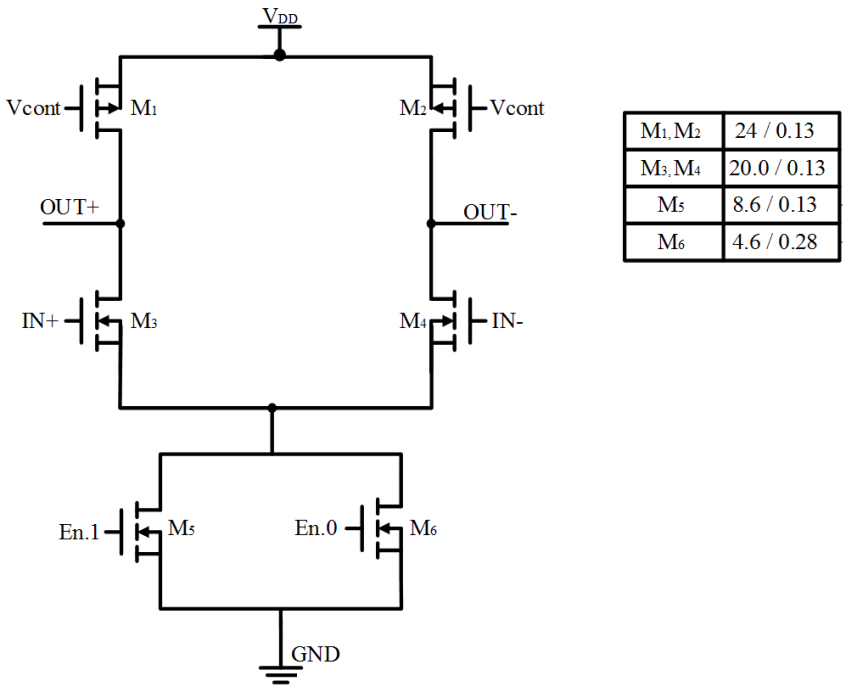


Figure 5. The four-phase LO generator block diagram.

3.4 RF Power Amplifier

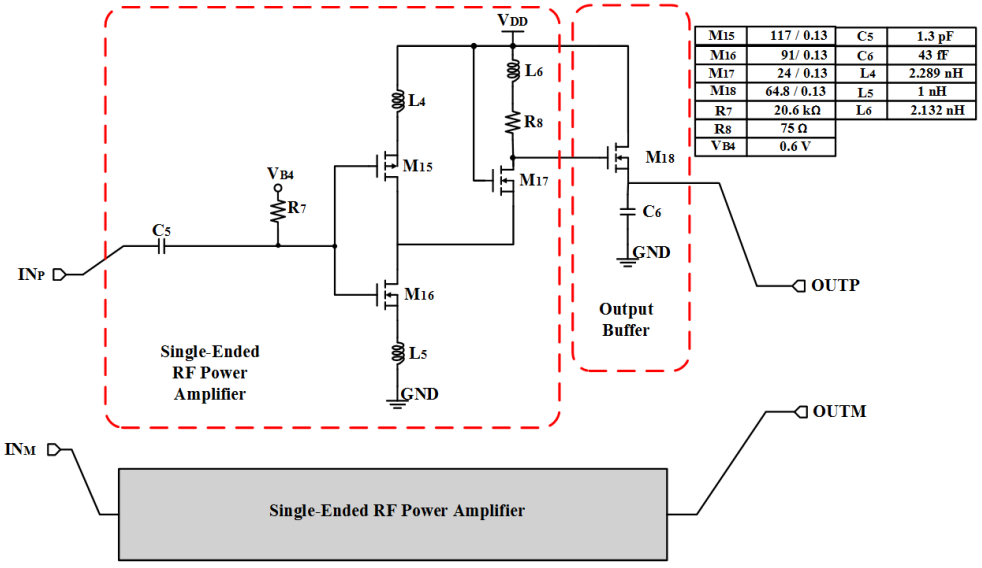
The circuit diagram of the RF power amplification stage is shown in Figure 7. In each amplifier, M15 and M16 are used as an amplifier with source degenerative inductors L4 and L5. Also the current-reuse technique is applied to (M15, M16) so a larger gain is achieved without an increase in power consumption. C5 is used for DC blocking. M17 is a common-gate amplifier following the input stage. Its main purpose is biasing the drains of (M15, M16), so that both stay in the saturation region. Inductance peaking techniques are also used here to improve the operating frequency [11]. M18 is designed as a buffer to drive a 50 ohm output load for the measurement purpose, and C6 represents the output pad parasitic capacitance. A single power amplifier and its output buffer drain 7.625 mA from a 1.2 V power supply.

"A 1.2-V Low-power Full-band Low-power UWB Transmitter with Integrated Quadrature Voltage-controlled Oscillator and RF Amplifier in 130nm CMOS Technology", Fadi R. Shahroury.



M1, M2	24 / 0.13
M3, M4	20.0 / 0.13
M5	8.6 / 0.13
M6	4.6 / 0.28

Figure 6. The simplified schematic diagram of unit differential delay cell.



M15	117 / 0.13	C5	1.3 pF
M16	91/ 0.13	C6	43 fF
M17	24 / 0.13	L4	2.289 nH
M18	64.8 / 0.13	L5	1 nH
R7	20.6 kΩ	L6	2.132 nH
R8	75 Ω		
VB4	0.6 V		

Figure 7. The simplified schematic diagram of RF power amplifier.

4. SIMULATION RESULTS

The proposed UWB transmitter with on-chip QVCO was designed, simulated and verified using Cadence Spectre Circuit Simulator in TSMC 130nm 1P8M CMOS technology. It consumes a total power of 77.8 mW. The transmitter covers the 14 bands of UWB MB-OFDM system, so that it can be used for UWB full-band application.

The design and optimization of UWB transmitter require precise RF modeling for both active and passive devices over a wide range of operation. Thus, in our simulation, we have used the RF models extracted from the physical layout.

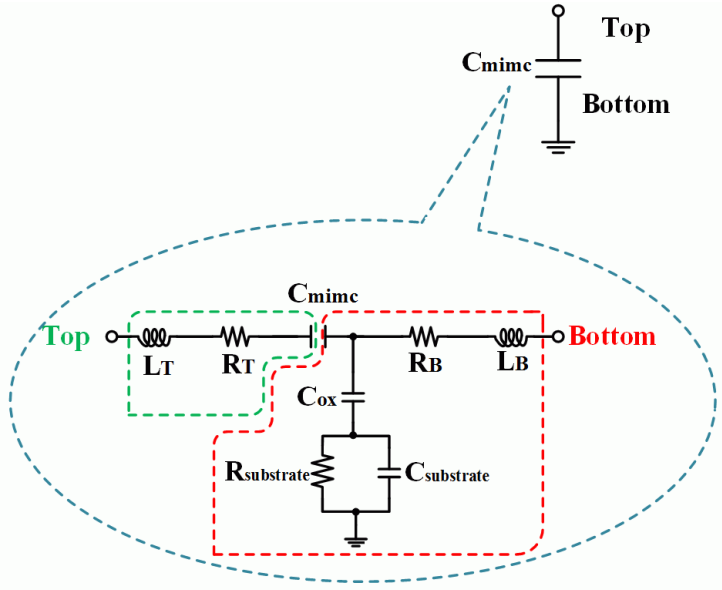


Figure 8. The RF model of the capacitor.

The capacitor RF model is shown in Figure 8. The main capacitance in the model is C_{mimc} which has two plates: the top plate and the bottom plate. Between the main capacitor and the top plate, there will be a parasitic inductance (L_T) and resistance (R_T), as well as on the bottom plate side (L_B) and (R_B). Since the bottom plate is close to the silicon substrate, this will create an oxide capacitance modeled as C_{OX}. $R_{substrate}$ and $C_{substrate}$ present the silicon substrate resistance and capacitance, respectively.

The QVCO tuning curves for the typical process are shown in Figure 9. From Figure 9, it can be seen that the QVCO covers all 14 bands in the UWB system. The QVCO works in two modes: the high frequency mode (when En.1 is enabled) which covers the frequency range from 3.28 GHz to 11.16 GHz and the low frequency mode (when En.1 is enabled) which covers the range from 1.5 GHz to 6.2 GHz. There is an overlap between each mode, which starts at 6.2 GHz and ends at 3.28 GHz with a total overlap of 2.9 GHz. This overlap is designed to be high enough in order to alleviate the frequency shift in the QVCO due to different corner processes (FF, SS, FS and SF). From the simulation, the critical cases for overlap frequency and QVCO frequency coverage range were in fast and slow process, as depicted in Figure 10 and Figure 11. From the results illustrated in Figure 10 and Figure 11, for fast and slow process, respectively, the QVCO still covers the entire band of the UWB system in both corners. The transient time simulation result of the proposed QVCO at 10 GHz under typical process is shown in Figure 12.

Table 1. The simulated power consumption in all circuit blocks of the proposed transmitter.

Transmitter	**Power**
QVCO	19.4 mW
Quadrature modulator core	40.1 mW
RF power amplifier	18.3 mW

Table 2. Performance and result comparison of published UWB transmitter.

	This work	[3]	[4]	[5]	[6]	[7]
Technology	130 nm CMOS	180 nm CMOS	90 nm CMOS	130 nm CMOS	130 nm CMOS	130 nm CMOS
Supply voltage	1.2 V	1.8 V	1.1 V	1.2 V	1.5 V	1.2 V
Bandwidth	2GHz-11GHz	3GHz-8GHz	3.1GHz-9.5GHz	3GHz-8GHz	3GHz-5GHz	3GHz-11GHz
Number of bands	14	9	12	9	3	14
OP_{-1dB}	4.35 dBm	–8.2 dBm	–2.8 dBm	1.5dBm	5 dBm	–0.4 dBm
Containing VCO	Yes	No	No	No	No	No
Power	77.8 mW	139 mW	131 mW	66 mW	97.5 mW	53.1 mW

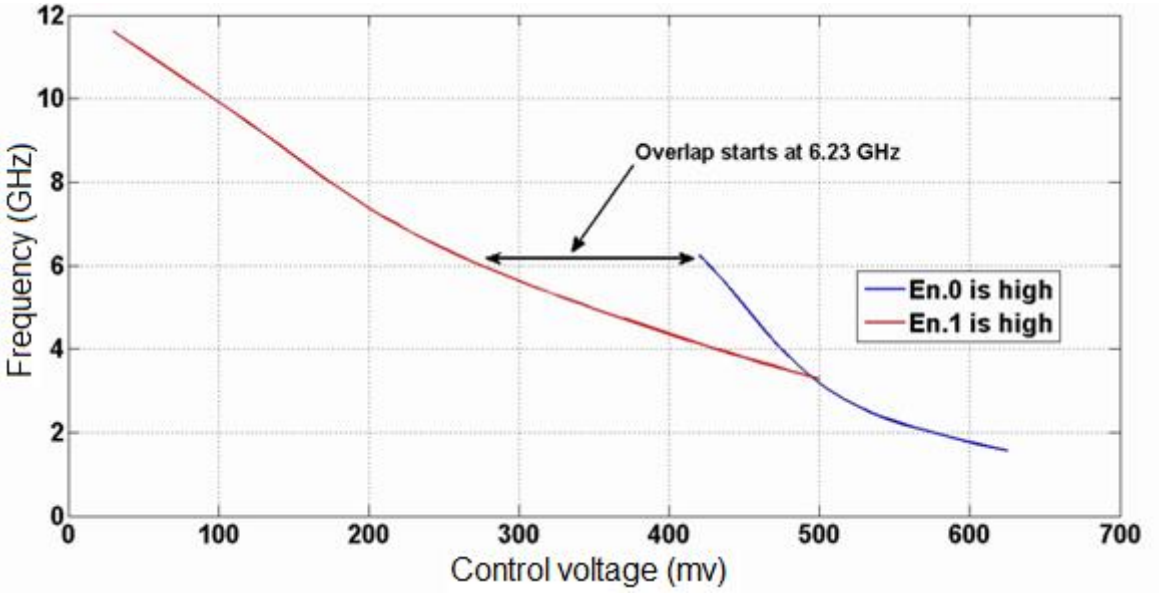


Figure 9. QVCO tuning curves, typical process.

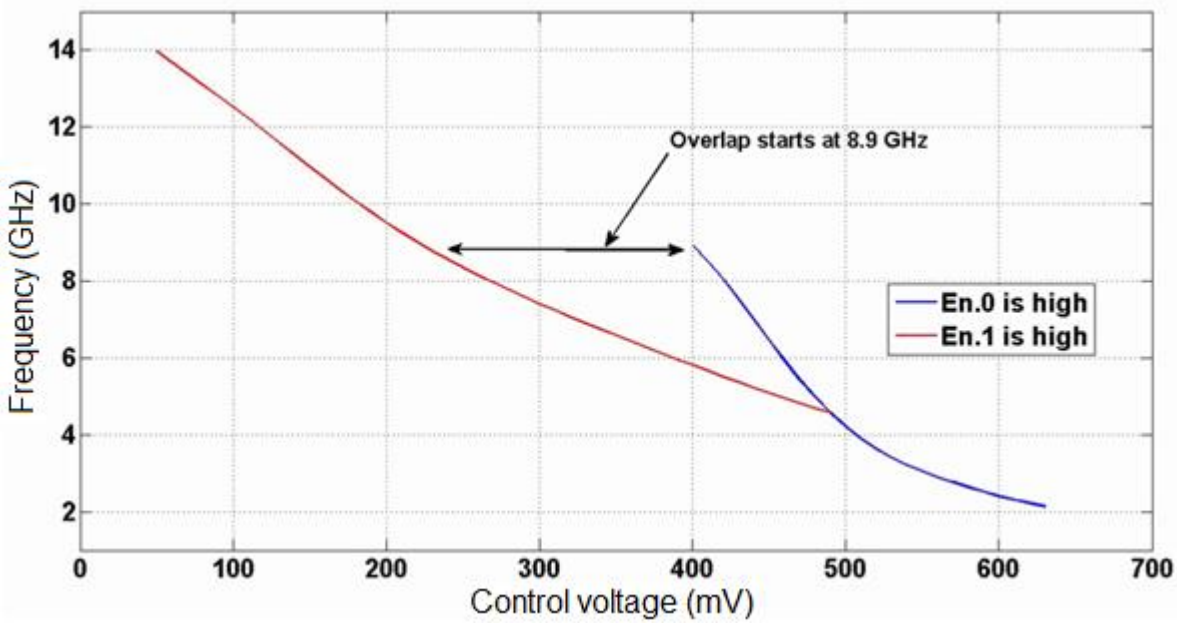


Figure 10. QVCO tuning curves, fast process.

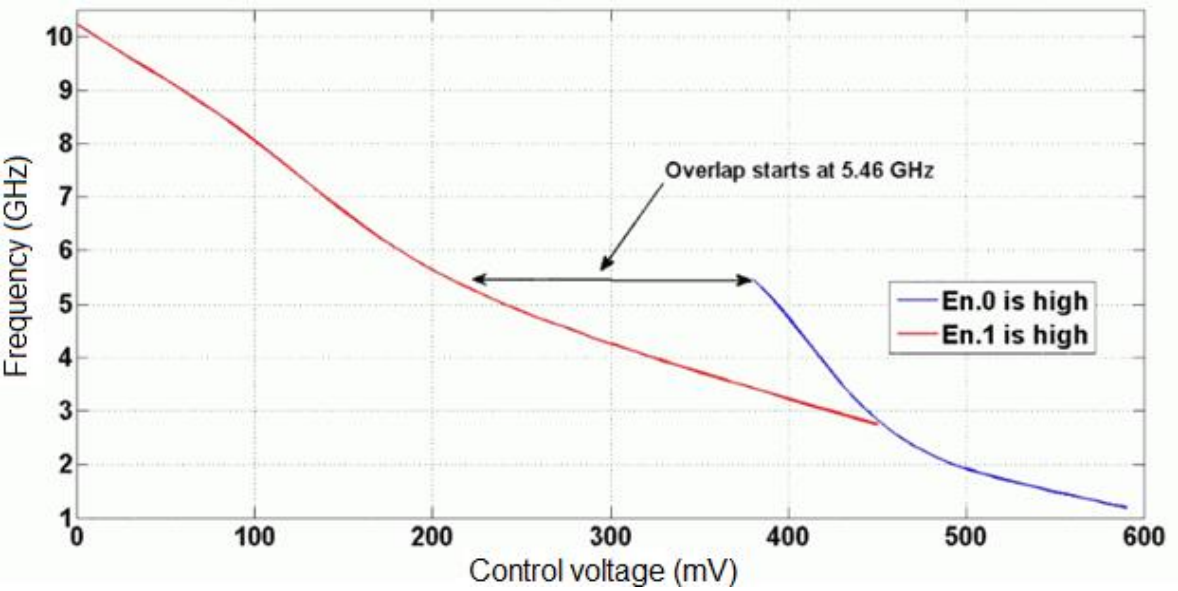


Figure 11. QVCO tuning curves, slow process.

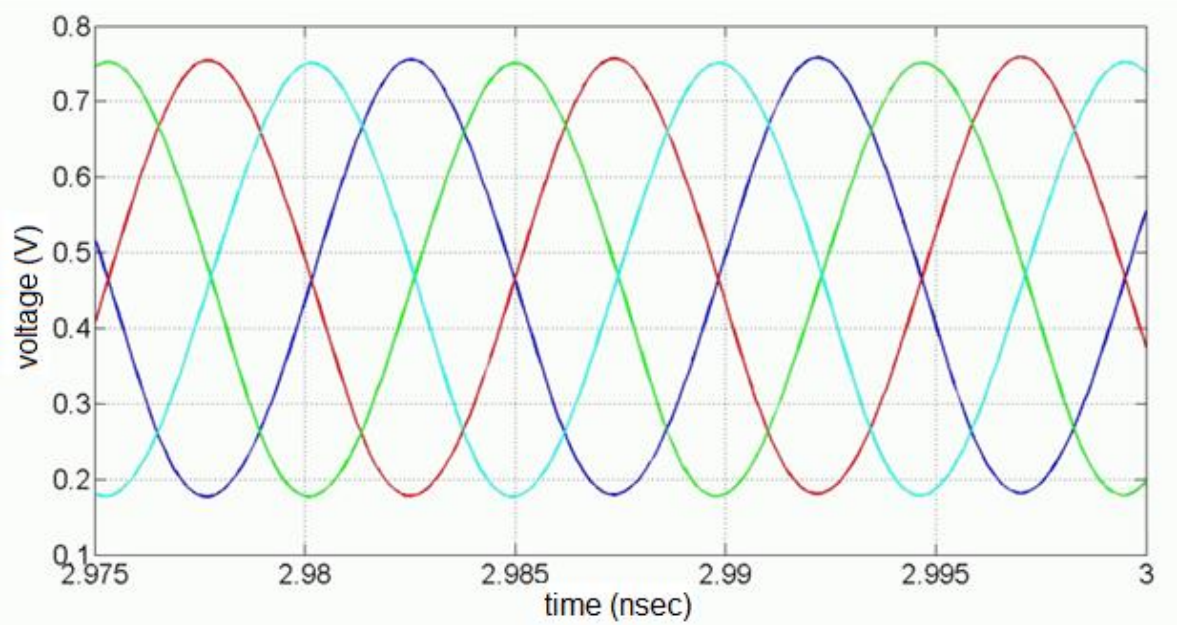


Figure 12. The transient time simulation of QVCO at 10 GHz for typical process, 25°C, $V_{cont.}$ = 0 V.

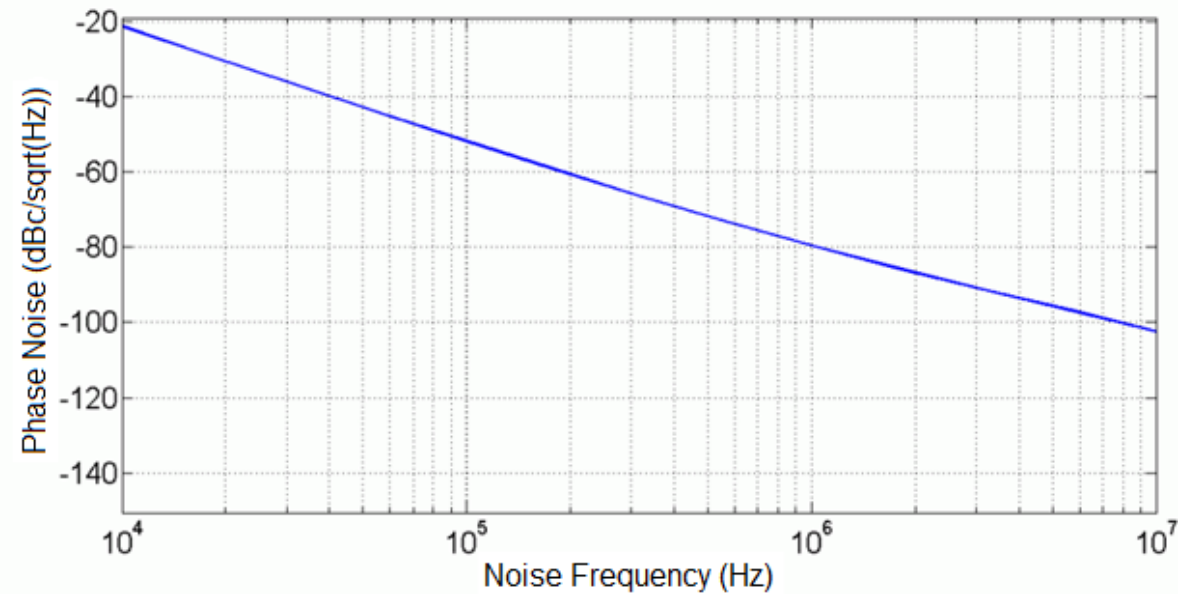


Figure 13. The simulated phase noise of the QVCO.

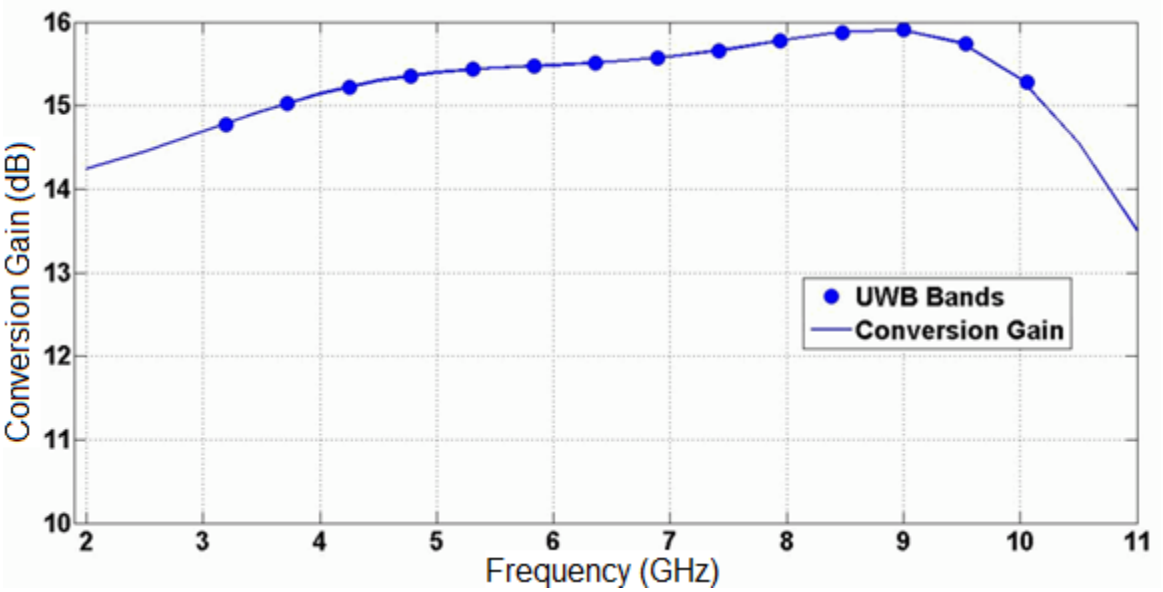


Figure 14. The simulated UWB transmitter conversion gain.

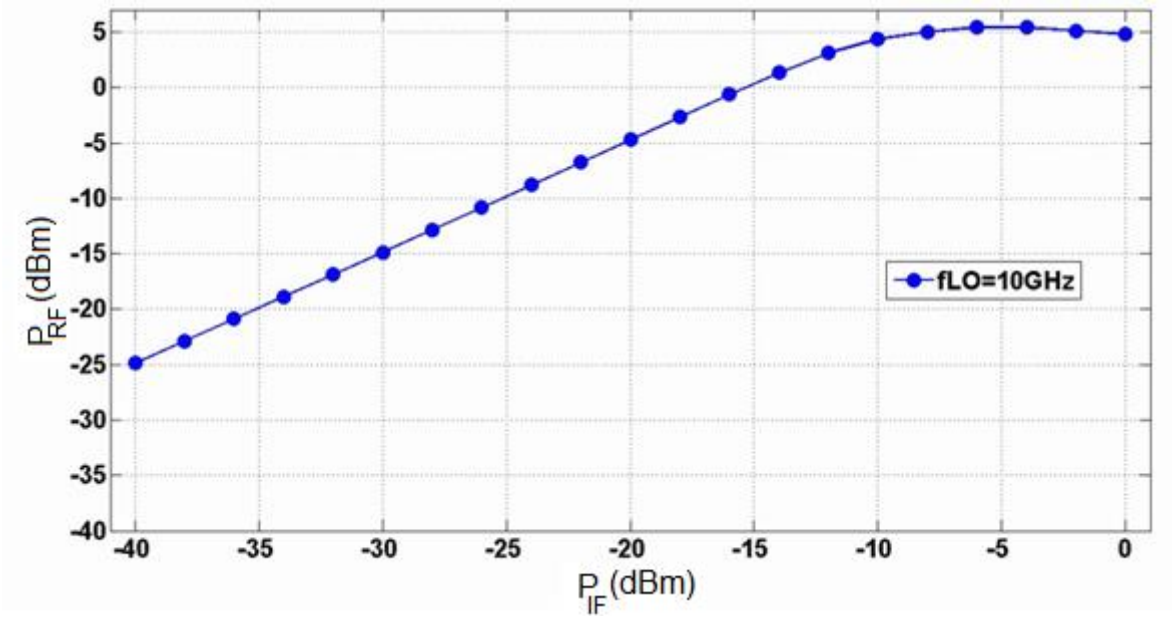


Figure 15. Linearity performance of the UWB transmitter at 10 GHz.

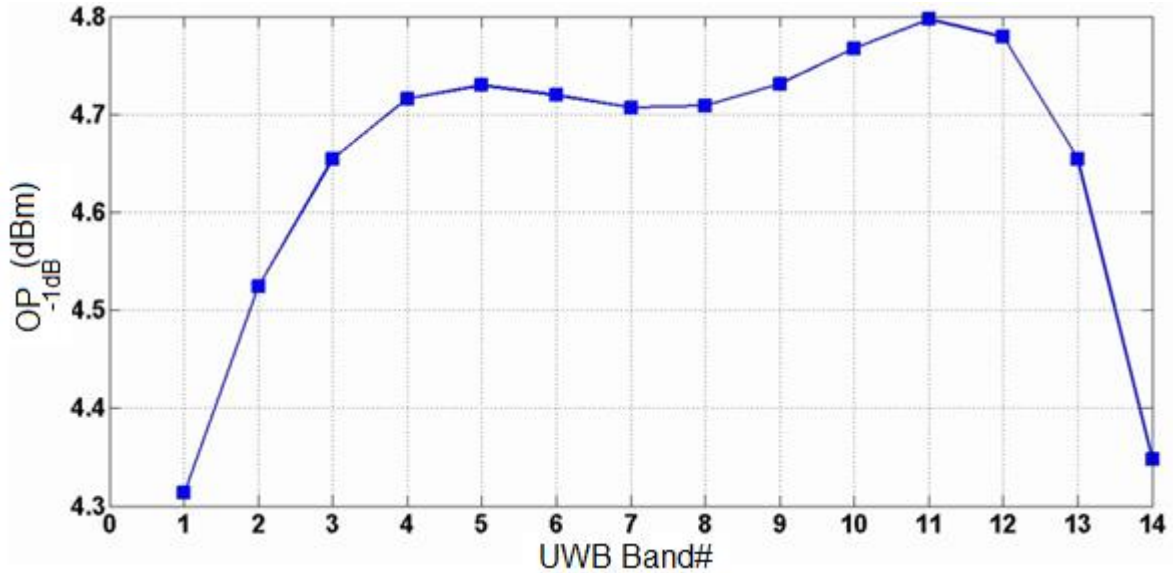


Figure 16. The simulated OP1dB of the UWB transmitter over each band.

The simulated phase noise of the proposed QVCO is shown in Figure 13. The worst case for phase noise of QVCO is –80 dBc at 1 MHz offset frequency with an operating frequency of 11 GHz.

The transmitter conversion gain in the frequency range from 2 GHz to 11 GHz is shown in Figure 14. As can be seen from Figure 14, the simulated average conversion gain of 15.28 dB is achieved with a gain ripple of ±1dB.

The simulated output power (PRF) *versus* the input IF power (PIF) is shown in Figure 15, where the corresponding IP1dB and OP1dB are –10 dBm and 4.35 dBm, respectively. The average simulated OP1dB is 4.65 dBm over the entire 14 bands as depicted in Figure 16.

The power consumption of each circuit block is shown in Table 1, while the simulated performance parameters are summarized in Table 2. In addition, comparisons with other published works are listed. Based upon Table 2, it is clear that the proposed transmitter with implemented QVCO covers the full-band of MB-OFDM (2 GHz-11 GHz) under low power dissipation. It drains 64.83 mA from the supply voltage of 1.2 V. Besides, the OP1dB achievement of the proposed UWB transmitter is the highest except [6], and it conforms with the specifications of UWB applications [12].

5. CONCLUSION

In this paper, a UWB full-band MB-OFDM transmitter with implemented QVCO is designed. The transmitter covers the frequency range from 2 GHz to 11 GHz and can cover all of the frequency bands of the UWB MB-OFDM system (14 bands) due to the use of inductance peaking technique. The simulation results have shown that the proposed transmitter can achieve a conversion gain of 15.28 dB with a ripple of ±1dB. In addition, the power dissipation of the proposed transmitter is 77.8 mW from a 1.2 V supply voltage. Future search will be conducted on the design of frequency synthesizer to reduce the QVCO phase noise and to control the output frequency [12]. In addition, the carrier leakage and the sideband suppression of the proposed transmitter will be explored.

ACKNOWLEDGMENT

The author would like to thank EUROPRACTICE for their kind support by providing the Cadence Spectre Circuit Simulator and the technology files.

REFERENCES

[1] R. J. Fontana, "Recent System Applications of Short-pulse Ultra-wideband (UWB) Technology," IEEE Transactions on Microwave Theory and Techniques, vol. 52, pp. 2087-2104, 2004.

[2] F. W. Chia-Chin Chong and H. Inamura, "Potential of UWB Technology for the Next Generation Wireless Communications," in: Proc. IEEE 9th International Symposium on Spread Spectrum Techniques and Applications, Manaus-Amazon, pp. 422-429, 2006.

[3] D. L. C. S. Hui Zheng, S. Lou and L. Tatfu Chan, "A 3.1 GHz-8.0 GHz Single-Chip Transceiver for MB-OFDM UWB in 0:18m CMOS Process," IEEE Journal of Solid-State Circuits, vol. 44, pp. 414-426, 2009.

[4] H. K. A. Tanaka, H. Okada and H. Ishikawa, "A 1.1V 3.1 GHz-9.5GHz MB-OFDM UWB Transceiver in 90nm CMOS," in: Proc. IEEE International Solid-State Circuits Conference, p.398-407, San Francisco, CA, 2006.

[5] H.-Y. Shih and C.-W. Wang, "A Highly-Integrated 38 GHz Ultra-Wideband RF Transmitter with Digital-Assisted Carrier Leakage Calibration and Automatic Transmit Power Control," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 20, pp. 1357-1367, 2012.

[6] E. A. C. Sandner, "A WiMedia/MBOA-Compliant CMOS transceiver for UWB," IEEE Journal of Solid-State Circuits, vol. 41, pp. 2787-2794, 2006.

[7] Y.-K. L., Z.-D. H., Fadi R. Shahroury, Wen-Chieh Wang, Chang-Ping Liao and C.-Y. Wu, "The Design of Integrated 3-GHz to 11-GHz CMOS Transmitter for Full-Band Ultra-Wideband (UWB) Applications," in: Proc. IEEE International Symposium on Circuits and Systems, Seattle, WA, pp. 2709-2712, May 2008.

[8] W. Alliance, "Multi-band OFDM Physical Layer Specication," WiMedia Alliance, Tech. Rep. Release 1.1, 2005.

[9] B. Gilbert, "A Precise Four Quadrant Multiplier With Sub-nanosecond Response," IEEE Journal of Solid-State Circuits, vol. 3, pp. 365-373, 1968.

[10] C.-Y. Chou and C.-Y. Wu, "The Design of Wideband and Low-power CMOS Active Polyphase Filter and Its Application in RF Double Quadrature Receiver," IEEE Transactions on Circuits and Systems I, vol. 52, pp. 825-833, May 2005.

[11] T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Second Edition, 2003.

[12] E. A. B. Razavi, "A UWB CMOS Transceiver," IEEE Journal of Solid-State Circuits, vol. 40, pp. 2555-2562, 2005.

ملخص البحث:

تقدم هذه الورقة البحثية تصميماً ومحاكاةً لمرسلٍ منخفض القدرة كامل النطاق في مجال النطاق فائق الاتساع (UWB) مع مذبذب رباعي مُتحكّم به بفرق الجهد (QVCO)، يستخدم تكنولوجيا أشباه الموصلات ذات الأكسيد المعدني المتممة (CMOS)/130 نانومتراً. ويتكوّن المرسل المقترح من مرشح سلبي متعدد الأطوار (PPF)، ومذبذب رباعي مُتحكَّم به بفرق الجهد (QVCO)، وقلب معدِّل رباعي، ومضخم قدرة للإشارات ذات الترددات الراديوية (RF).

ويستخدم المذبذب بنية خلايا التأخير التفاضلية بأربع مراحل متعاقبة. ويمتلك المرسل المقترح المواصفات الآتية: كسب تحويل متوسط مقداره 15.28 ديسيبل بتعرُّج مقداره ± 1 ديسيبل في النطاق الترددي الممتدّ من 2 جيجاهيرتز إلى 11 جيجاهيرتز؛ نقطة ضغط الدّخل (IP1dB) تساوي -10 ديسيبل (dBm)؛ نقطة ضغط الخرج (OP1dB) تساوي 4.35 ديسيبل (dBm).

ويحقق المذبذب مدى ترددياً واسعاً يتراوح من 2 جيجاهيرتز إلى 11 جيجاهيرتز بضجيج طور مقداره -80 ديسيبل (dBc)/هيرتز. إضافة إلى ذلك، فإن فرق جهد التشغيل للمرسل المقترح يبلغ 1.2 فولت، في حين تبلغ القدرة التي يستهلكها 77.8 ميلي واط.